LOW COST, HIGH DENSITY DIFFUSION DIODE-CAPACITOR

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TECHNICAL FIELD

The present invention is directed to a high density junction capacitor structure that is formed utilizing a single mask and a series of angled ion implants resulting in an inter-digitated capacitor with superior diode breakdown, forward resistance and capacitance density characteristics.

BACKGROUND OF THE INVENTION

PN junctions are commonly used in semiconductor integrated circuits as diode-capacitor elements. The depletion layer of a PN junction is the interface of the junction and, as the name implies, is depleted of charge carriers. Under certain bias conditions, the depletion layer of a PN junction is capable of storing charge carriers. The capacitance of the depletion layer is proportional to its area. That is, for a given set of bias conditions, the greater the area occupied by the PN junction, the greater the capacitance. Of course, may integrated circuit applications require that the die size of the circuit be as small as possible. Therefore, it would be highly desirable to have available a PN junction capacitor structure that provides increased capacitance while utilizing smaller area.

A capacitor with an increased capacitance per unit area and for a given voltage range of operation is thus a valuable device. Capacitors with higher levels of doping offer a higher per unit area capacitance, but trade off breakdown voltage. Thus, a valuable device would offer both a high per unit area capacitance and a high breakdown voltage. A capacitor with a high breakdown voltage and a high per unit area capacitance is currently not readily available as a single PN junction.

DESCRIPTION OF THE DRAWINGS

Fig. 1 is a partial cross-section drawing illustrating a multi-layer diffusion junction capacitor structure in accordance with the concepts of the present invention.

DESCRIPTION OF THE INVENTION

The present invention provides a stack of interdigitated capacitors that are linked together by utilizing a tilted implant, thereby providing a capacitor structure with both a high capacitance per unit area and a high breakdown voltage, utilizing only a single mask.

Fig. 1 shows a multi-layer diffusion junction capacitor structure 100 formed in a semiconductor substrate 102. Typically, the semiconductor substrate 102 will be crystalline silicon, although other semiconductor materials (e.g. SiGe, Ge) can also be used. The capacitor structure 100 includes an N-type region 104 formed in the semiconductor substrate 102 and including a N-type vertical portion 104a and a plurality of spaced-apart N-type fingers 104b that extend from the N-type vertical portion 104a. The capacitor structure 100 also includes a P-type region 106 that includes a P-type vertical portion 106a and a plurality of spaced-apart P-type fingers 106b that extend from the P-type vertical portion 106a. As illustrated in Fig. 1, the combination of the N-type region 104 and the P-type region 106 results in a structure wherein the N-type fingers 104b and the P-type fingers 106b are inter-digitated.

The diode capacitor structure 100 shown in Fig. 1 can be formed in accordance with the following sequence of conventional semiconductor integrated circuit fabrication steps.

First, a patterned hard mask 108 is formed on an upper surface of the semiconductor substrate 102. The hard mask 108 may be formed using, for example, oxide, nitrite or photoresist. At least one opening 110 is formed in the hard mask 108 to expose an upper surface area 102a of the semiconductor substrate 102. Care is taken to control the angle of the sidewalls of the opening 110 in the hard mask 108 with the use of a dry, anisotropic etching process so that the sidewall is substantially vertical.

Next, a sequence of implant steps is performed wherein P-type (p+)and N-type (n+) dopant are alternatingly implanted at positive and negative implant angles, respectively. For a particular conductivity type dopant, each implant in the sequence is performed with a

different energy and implant dose, thereby resulting in the inter-digitated structure 100 shown in Fig. 1.

For example, in an embodiment of the invention, an oxide mask is formed on the upper surface of a silicon substrate. An opening is then formed in the oxide mask to expose an upper surface area of the silicon. Next, a phosphorous implant at a dose of 1 E13/cm^3 and at an implant energy of 15 KeV and at a tilt angle of -2 degrees is performed. This is followed by an implant of boron dopant at a dose of 8E11/cm^3 and an implant energy of 20 KeV and a tilt angle of 2 degrees. A second phosphorous implant is then performed at a dose of 5E11/cm^3 , an implant energy of 200 KeV and a tilt angle of -1 degree. A second boron implant is then performed at a dose of 3E11/cm^3 , an energy of 180 KeV and a tilt angle of 2 degrees. A third phosphorous implant is then performed at dose of 5E11/cm^3 , an implant energy of 600 KeV and a tilt angle of -2 degrees. A third boron implant is then performed at a dose of 6E11/cm^3 , an implant energy of 600 KeV and a tilt angle of 2 degrees. The preceding sequence of alternating phosphorous and boron implants results in a three layer inter-digitated diffusion diode/capacitor structure in accordance with the concepts of the present invention (see Fig. 1).

Following the formation of the inter-digitated capacitor structure, a layer of aluminum or other conductive interconnect material is deposited over the capacitor structure and etched to provide a conductive contact to the N-type dopant region 104 (see Fig. 1) and a conductive contact to the P-type dopant region 106 (see Fig. 1).

Although only specific embodiments of the present invention are shown and described herein, the invention is not to be limited by these embodiments. Rather, the scope of the invention is to be defined by these descriptions taken together with the attached claims and their equivalents.